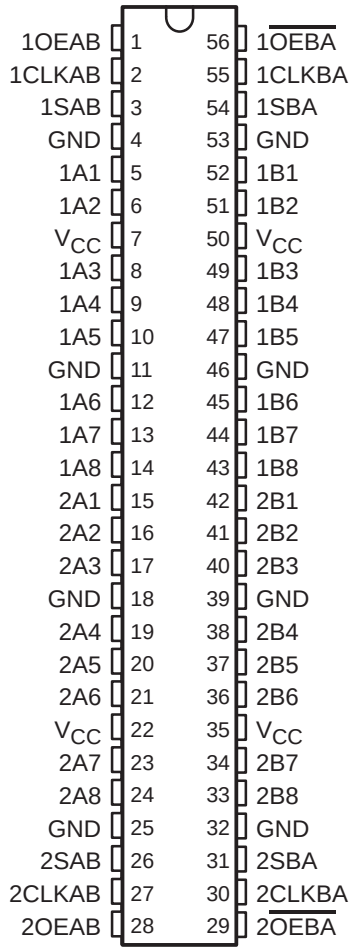
- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **Inverting Data Paths**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed $V_{CC}$ and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

**SN54ACT16651 . . . WD PACKAGE**
**74ACT16651 . . . DL PACKAGE**
**(TOP VIEW)**




## description

The SN54ACT16651 and 74ACT16651 are 16-bit bus transceivers that consist of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN54ACT16651 and 74ACT16651.

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## description (continued)

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The 74ACT16651 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

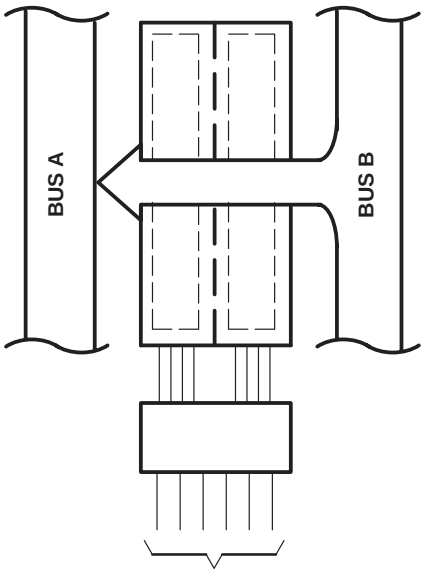
The SN54ACT16651 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16651 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| L | H | L | L | X | X | Input | Input | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | L | X | X | Input | Unspecified‡ | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | L | ↑ | X | X | Unspecified‡ | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time $\overline{\text{B}}$ data to A bus |
| L | L | X | L | X | H | Output | Input | Stored $\overline{\text{B}}$ data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time $\overline{\text{A}}$ data to B bus |
| H | H | L | X | H | X | Input | Output | Stored $\overline{\text{A}}$ data to B bus |
| H | L | L | L | H | H | Output | Output | Stored $\overline{\text{A}}$ data to B bus and stored $\overline{\text{B}}$ data to A bus |

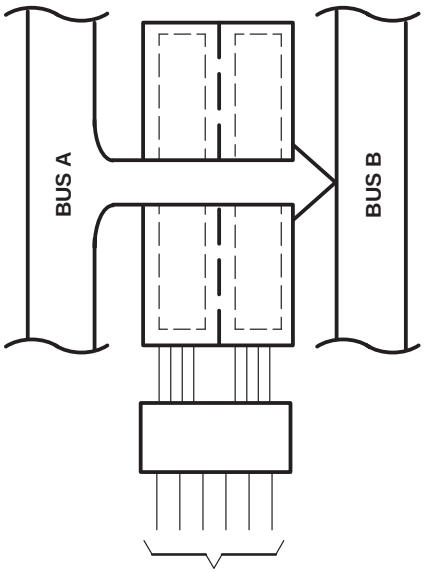
† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered to load both registers.



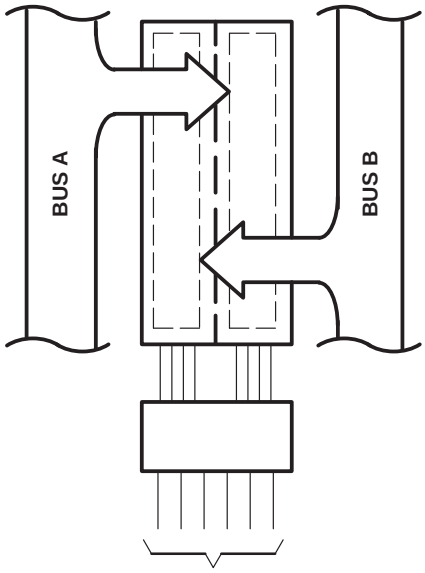

| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**



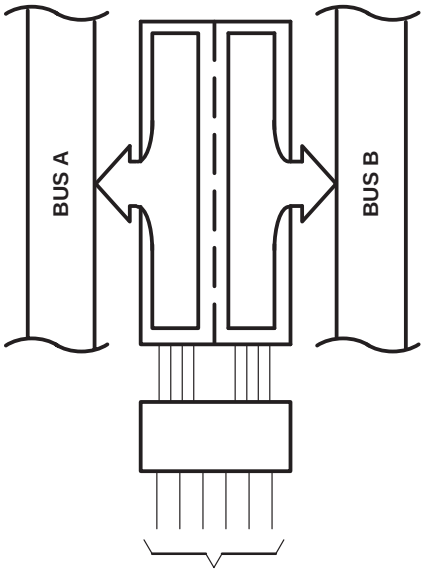

| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**




| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**

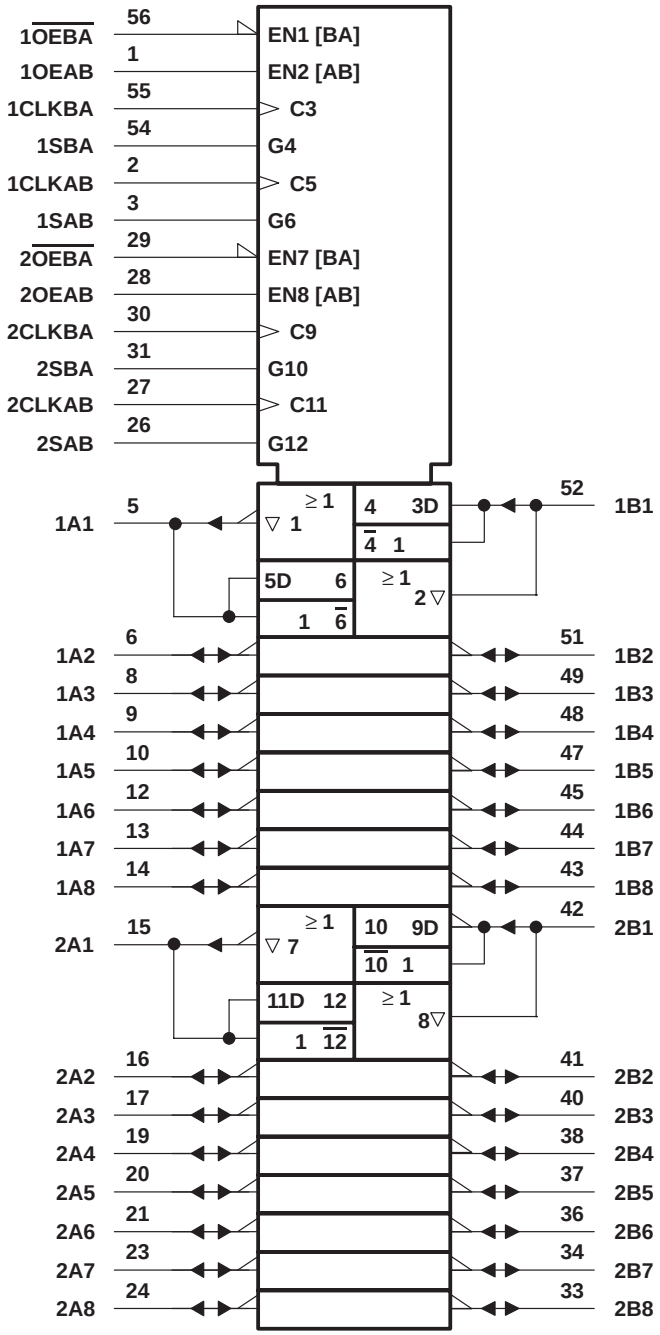



| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | L | L | L | H | H |

**TRANSFER STORED DATA**
**TO A AND/OR B**

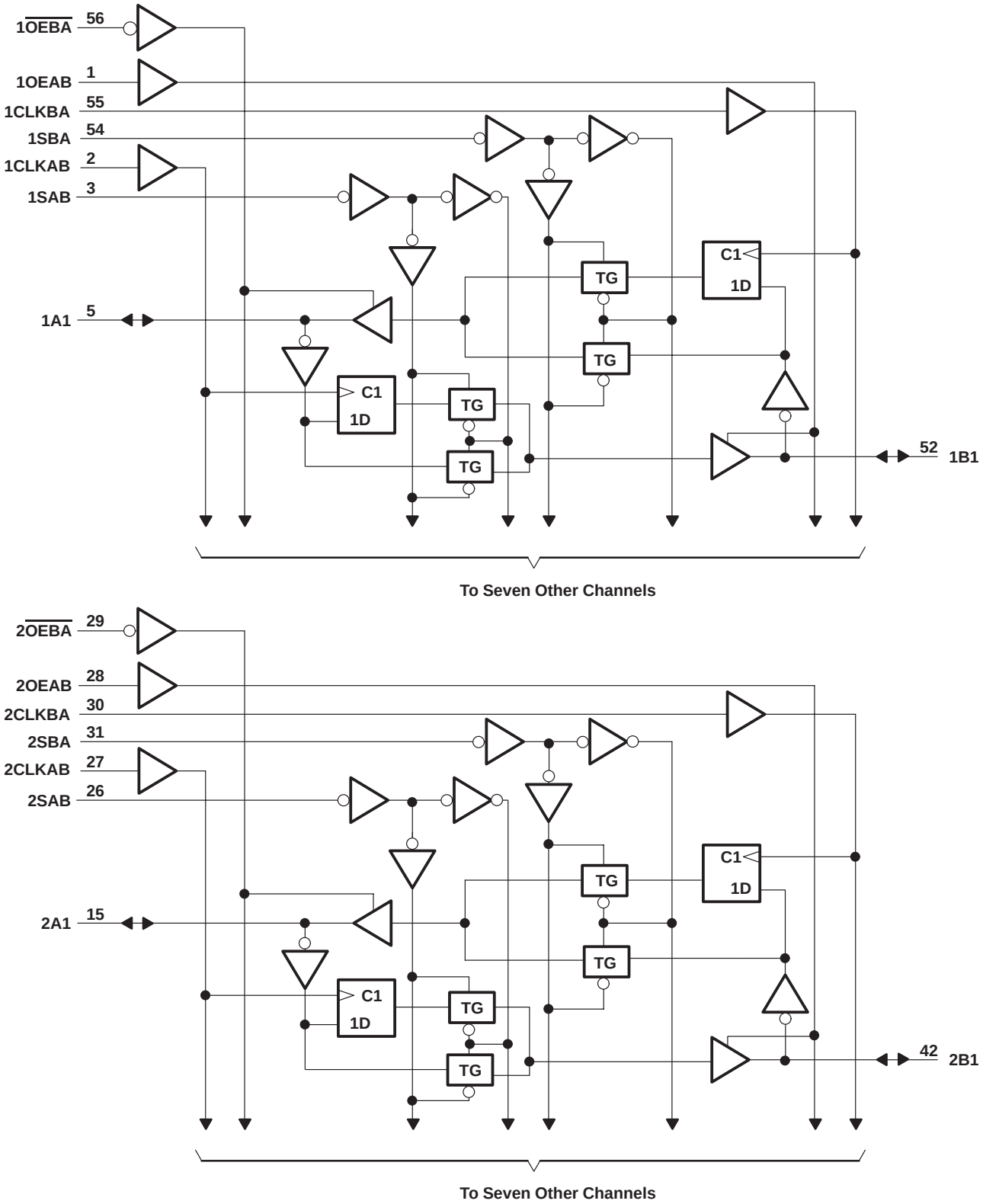
**Figure 1. Bus-Management Functions**

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±400 mA
Maximum package power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DL package . . . . . 1.4 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

### recommended operating conditions (see Note 3)

| | | SN54ACT16651 | | | 74ACT16651 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | | | –24 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | | 10 | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | | 125 | –40 | | 85 | °C |

PRODUCT PREVIEW

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54ACT16651 | | 74ACT16651 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | V |
| | | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | | $I_{OH}$ = –24 mA | 4.5 V | 3.94 | | | 3.7 | | 3.8 | | |
| | | | 5.5 V | 4.94 | | | 4.7 | | 4.8 | | |
| | | $I_{OH}$ = –50 mA† | 5.5 V | | | | 3.85 | | | | |
| | | $I_{OH}$ = –75 mA† | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 5.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50 mA† | 5.5 V | | | | | 1.65 | | | |
| | | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | | 1.65 | |
| $I_I$ | Control inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{OZ}$‡ | A or B ports | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.5 | | ±10 | | ±5 | µA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 8 | | 160 | | 80 | µA |
| $\Delta I_{CC}$§ | | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 0.9 | | 1 | | 1 | mA |
| $C_i$ | Control inputs | $V_I = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O = V_{CC}$ or GND | 5 V | | 12 | | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

| | | $T_A$ = 25°C | | SN54ACT16651 | | 74ACT16651 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | 0 | 90 | 0 | 90 | 0 | 90 | MHz |
| $t_w$ | Pulse duration, CLKAB or CLKBA high or low | 5.5 | | 5.5 | | 5.5 | | ns |
| $t_{su}$ | Setup time, A before CLKAB↑ or B before CLKBA↑ | 5.3 | | 5.3 | | 5.3 | | ns |
| $t_h$ | Hold time, A after CLKAB↑ or B after CLKBA↑ | 1 | | 1 | | 1 | | ns |

PRODUCT PREVIEW

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## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | SN54ACT16651 | | 74ACT16651 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 90 | | | 90 | | 90 | | MHz |
| $t_{PLH}$ | A or B | B or A | 3 | 6.6 | 10 | 3 | 12.2 | 3 | 11.3 | ns |
| $t_{PHL}$ | | | 4.6 | 8 | 10.6 | 4.6 | 12.7 | 4.6 | 11.9 | |
| $t_{PLH}$ | CLKBA or CLKAB | A or B | 5.4 | 9.1 | 12 | 5.4 | 14.8 | 5.4 | 13.7 | ns |
| $t_{PHL}$ | | | 5.4 | 9.1 | 12 | 5.4 | 14.6 | 5.4 | 13.6 | |
| $t_{PLH}$ | SBA or SAB (with A or B high) | A or B | 4.6 | 7.9 | 10.5 | 4.6 | 13.1 | 4.6 | 12.1 | ns |
| $t_{PHL}$ | | | 5.4 | 10.9 | 15.5 | 5.4 | 19.6 | 5.4 | 17.8 | |
| $t_{PLH}$ | SBA or SAB (with A or B low) | A or B | 5 | 10.4 | 14.9 | 5 | 19.2 | 5 | 17.3 | ns |
| $t_{PHL}$ | | | 4.9 | 8.6 | 11.9 | 4.9 | 13.7 | 4.9 | 12.7 | |
| $t_{PZH}$ | $\overline{OEBA}$ | A | 3.2 | 7.2 | 10.8 | 3.2 | 13.6 | 3.2 | 12.3 | ns |
| $t_{PZL}$ | | | 3.8 | 8 | 12.2 | 3.8 | 15.3 | 3.8 | 13.9 | |
| $t_{PHZ}$ | $\overline{OEBA}$ | A | 5.1 | 7.8 | 9.8 | 5.1 | 11.3 | 5.1 | 10.6 | ns |
| $t_{PLZ}$ | | | 4.9 | 7.7 | 9.9 | 4.9 | 11.4 | 4.9 | 10.8 | |
| $t_{PZH}$ | OEAB | B | 4.9 | 8 | 10.5 | 4.9 | 12.9 | 4.9 | 11.9 | ns |
| $t_{PZL}$ | | | 5.4 | 8.8 | 11.8 | 5.4 | 14.7 | 5.4 | 13.5 | |
| $t_{PHZ}$ | OEAB | B | 4.3 | 7.5 | 10.7 | 4.3 | 12 | 4.3 | 11.4 | ns |
| $t_{PLZ}$ | | | 4.5 | 7.6 | 10.8 | 4.5 | 12.3 | 4.5 | 11.6 | |

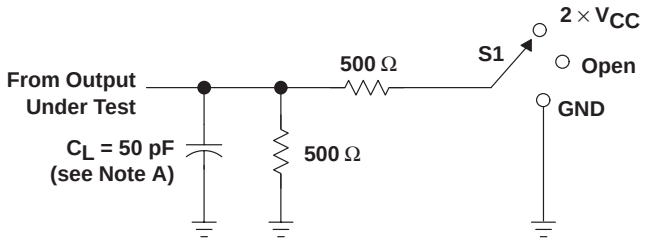
PRODUCT PREVIEW

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per transceiver | Outputs enabled | $C_L$ = 50 pF, f = 1 MHz | 62 | pF |
| | | Outputs disabled | | 14 | |

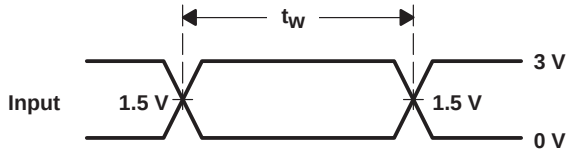
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## PARAMETER MEASUREMENT INFORMATION

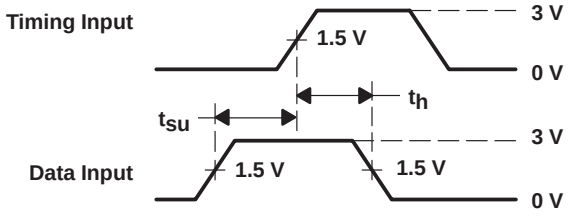



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

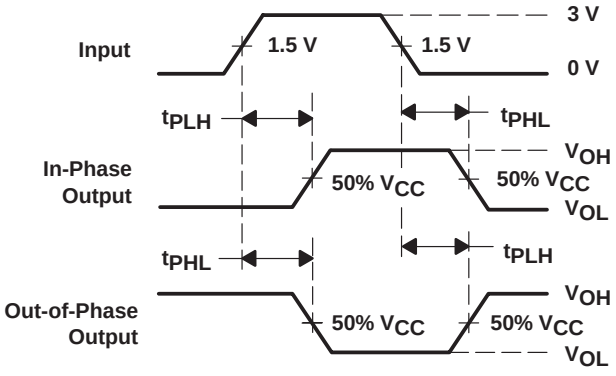
LOAD CIRCUIT



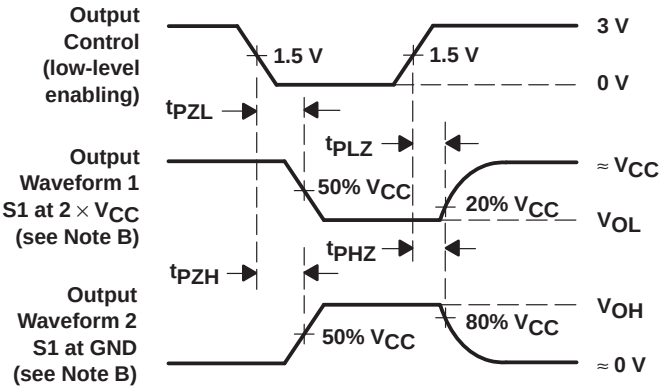

VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 74ACT16651DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ACT16651DLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ACT16651DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ACT16651DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

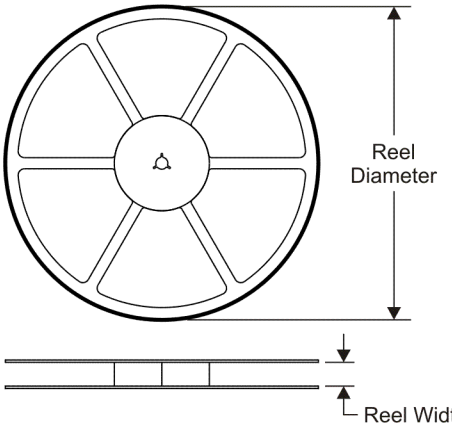
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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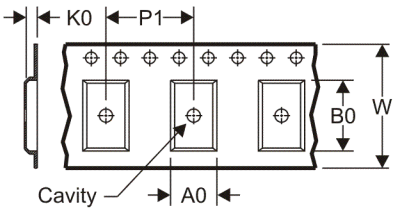
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

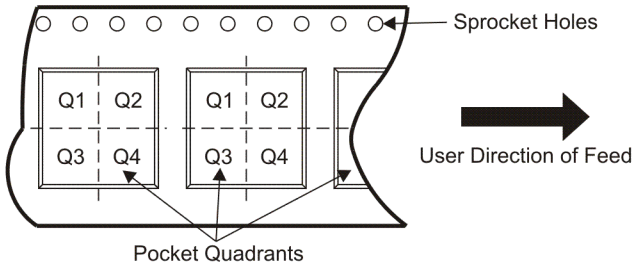



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

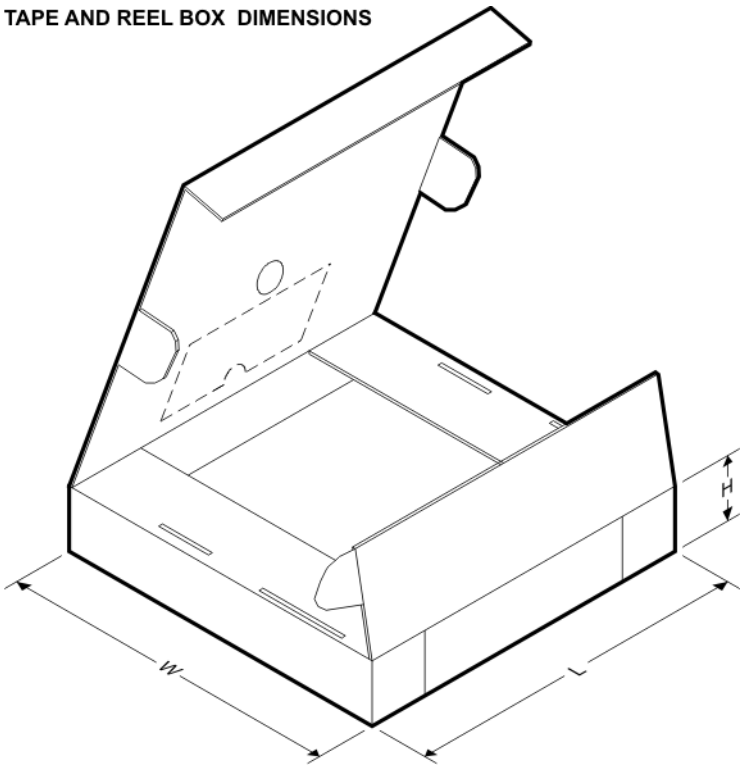
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74ACT16651DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74ACT16651DLR | SSOP | DL | 56 | 1000 | 346.0 | 346.0 | 49.0 |

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